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FINDLEY, CHRISTOPHER G

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NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com.tw

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *8/19/2008*.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-34* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-34* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____ .

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments, see page 11, line 17 through page 12,line 12, filed

8/19/2008, with respect to the rejection(s) of claim(s) 1-3, 12-15, 23-26, 29, and 32-33

under 35 U.S.C. 102(e) as being anticipated by Nakaya (US 7006571 B1, hereafter

referred to as "'6571") have been fully considered and are persuasive. Therefore, the

rejection has been withdrawn. However, upon further consideration, a new ground(s) of

rejection is made under of 35 U.S.C. 103(a) in view of Nakaya '6571.

2.   Applicant's arguments filed 8/19/2008 regarding use of a single interpolation unit,

see page 12, line 14 through page 13, line 20, have been fully considered but they are

not persuasive. Fig. 11 of Nakaya '6571 corresponds to predicted image synthesizer

711 of Fig. 7. Predicted image synthesizer 711 accepts both global motion parameters

and block matching vector information extracted from the motion information 702 and

the appropriate final predicted image is synthesized according to the input motion

information type and output via connection 712 (Nakaya '6571:Fig. 7; column 14, lines

22-34). Therefore, the single predicted image synthesizer as a unit is capable of

performing either global motion compensation or block matching synthesis.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains.
Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 1-4, 12-15, 23-26, 29, and 32-34 are rejected under 35 U.S.C. 103(a)

as being unpatentable over Nakaya (US 7006571 B1, hereafter referred to as

"'6571").

Re **claim 1**, '6571 discloses an apparatus for performing motion compensation

when decoding an incoming video bit stream including a plurality of frames having first

macroblocks encoded using block-matching motion compensation (Nakaya '6571: Fig.

11/1101) and second macroblocks encoded using global motion compensation (Nakaya

'6571: Fig. 11/911), the apparatus comprising: an interpolation unit for performing

interpolation operations on each macroblock contained in each frame of the incoming

video stream (Nakaya '6571: column 13, lines 56-61; the images are synthesized

relative to the previously decoded images); wherein when processing a current

macroblock, if the current macroblock is encoded using block-matching motion

compensation, the interpolation unit performs the interpolation operations according to

the macroblock motion vector (Nakaya '6571: Fig. 11; column 15, lines 2-8, either the

global motion scheme or the block matching scheme is employed based on the

selection information extracted from the motion information and the appropriate

synthesizer feeds the predicted image into the switch for output); and if the current

macroblock is encoded using global motion compensation, the interpolation unit

performs the interpolation operations according to a global motion vector on a per-

macroblock basis (Nakaya '6571: Fig. 11; column 15, lines 2-8, either the global motion

scheme or the block matching scheme is employed based on the selection information

extracted from the motion information and the appropriate synthesizer feeds the

predicted image into the switch for output).

Nakaya '6571 does not specifically disclose a multiplexer selecting an inputted

macroblock motion vector or an inputted global motion vector and outputting the

selected macroblock motion vector or the selected global motion vector to the

interpolation unit. However, Nakaya '6571 does disclose a multiplexer with inputs

connected to the GMC predicted image synthesizer and the block matching predicted

synthesizer (Nakaya '6571: Fig. 11, multiplexer 908; column 15, lines 2-8, either the

global motion scheme or the block matching scheme is employed based on the

selection information extracted from the motion information and the appropriate

synthesizer feeds the predicted image into the switch for output). Although the

multiplexer disclosed by Nakaya '6571 inputs information from the synthesizer units, as

opposed to the claimed outputting motion vector data to the interpolation unit, one of

ordinary skill in the art at the time of the invention would have found it obvious that in

both the claimed configuration and the configuration described by Nakaya '6571, the

interpolation unit (embodied by the predicted image synthesizer 711 in Fig. 7 of Nakaya

'6571) receives either a global motion vector or block motion vector and generates a

predicted image. The configuration presented in the prior art, wherein the multiplexer

selects from either the global motion predicted image or the block matching predicted

image (Nakaya '6571: Fig. 11), inputs the appropriate vector type to the prediction units

(Nakaya '6571: Fig. 11, elements 904 and 907) and selects the appropriate input for the

multiplexer (Nakaya '6571: Fig. 11, element 909), assuring that the resultant predicted

image is interpolated with the proper motion type, yielding the same results as the

claimed configuration. Therefore, the surrounding elements in the decoding system,

such as the decoder shown in Fig. 7 of Nakaya '6571, would function the same

regardless of whether the predicted image synthesizer (Nakaya '6571: Fig. 7, element

711) conformed to the configuration shown in Fig. 11 of Nakaya '6571 or the

configuration claimed in the instant application, and, thus, there would be no invention in

shifting the position of the multiplexer, as claimed by the Applicant. See In re Japikse,

86 USPQ 70 (CCPA 1950).

Re **claim 2**, Nakaya '6571 discloses converting global motion information into

representative vectors (Nakaya '6571: Equations (5), (6), (7), and (8); the vector

components are calculated from motion information parameters).

Re **claim 3**, Nakaya '6571 discloses that when processing the current

macroblock, if the current macroblock is encoded using block-matching motion

compensation, the interpolation unit performs the interpolation operations according to

at least one macroblock motion vector contained in the current macroblock (Nakaya

'6571: Fig. 11; column 15, lines 2-8).

Re **claim 4**, as stated above in claim 1, Nakaya '6571 does not specifically

disclose a multiplexer selecting an inputted macroblock motion vector or an inputted

global motion vector and outputting the selected macroblock motion vector or the

selected global motion vector to the interpolation unit. However, Nakaya '6571 does

disclose a multiplexer with inputs connected to the GMC predicted image synthesizer

and the block matching predicted synthesizer (Nakaya '6571: Fig. 11, multiplexer 908;

column 15, lines 2-8, either the global motion scheme or the block matching scheme is employed based on the selection information extracted from the motion information and the appropriate synthesizer feeds the predicted image into the switch for output). Although the multiplexer disclosed by Nakaya '6571 inputs information from the synthesizer units, as opposed to the claimed outputting motion vector data to the interpolation unit, one of ordinary skill in the art at the time of the invention would have found it obvious that in both the claimed configuration and the configuration described by Nakaya '6571, the interpolation unit (embodied by the predicted image synthesizer 711 in Fig. 7 of Nakaya '6571) receives either a global motion vector or block motion vector and generates a predicted image. The configuration presented in the prior art, wherein the multiplexer selects from either the global motion predicted image or the block matching predicted image (Nakaya '6571: Fig. 11), inputs the appropriate vector type to the prediction units (Nakaya '6571: Fig. 11, elements 904 and 907) and selects the appropriate input for the multiplexer (Nakaya '6571: Fig. 11, element 909), assuring that the resultant predicted image is interpolated with the proper motion type, yielding the same results as the claimed configuration. Therefore, the surrounding elements in the decoding system, such as the decoder shown in Fig. 7 of Nakaya '6571, would function the same regardless of whether the predicted image synthesizer (Nakaya '6571: Fig. 7, element 711) conformed to the configuration shown in Fig. 11 of Nakaya '6571 or the configuration claimed in the instant application, and, thus, there would be no invention in shifting the position of the multiplexer, as claimed by the Applicant. See In re Japikse, 86 USPQ 70 (CCPA 1950).

Nakaya '6571 also does not specifically disclose that either the block matching motion vector or the global motion vector are stored to a vector storage unit. However, the Examiner takes Official Notice that it is conventional to store such data into a buffer so that the vectors are retained until the processing steps relating to each block are completed. Therefore, one of ordinary skill in the art would have found it obvious to store the vectors into a buffer so that, due to the complexity of the calculations involved, the vectors could still be used for processing in the event of an error.

Re **claim 12**, Nakaya '6571 discloses that when performing the interpolation operations, the interpolation unit uses a bilinear interpolation process (Nakaya '6571: column 3, lines 37-40).

Claim 13 is the corresponding method claim to the apparatus of claim 1 and has been analyzed and rejected with respect to claim 1 above.

Claim 14 has been analyzed and rejected with respect to claim 2 above.

Claim 15 has been analyzed and rejected with respect to claim 3 above.

Claim 23 has been analyzed and rejected with respect to claim 12 above.

Re **claim 24**, Nakaya '6571 discloses a predicted image synthesizer in a video decoder for decoding a video bit stream and generating a predicted image (Nakaya '6571: Fig. 7/711), the video bit stream including a plurality of frames having first macroblocks encoded using block-matching compensation (Nakaya '6571: Fig. 11/1101) and second macroblocks encoded using global motion compensation (Nakaya '6571: Fig. 11/911) , the video bit stream including macroblock motion vectors indicating motion vectors of the first macroblocks (Nakaya '6571: column 14, line 64, through

column 15, line 2) and global motion parameters associated with the plurality of frames

indicating a motion vector of each pixel in the second macroblocks (Nakaya '6571:

column 14, lines 58-64), the predicted image synthesizer comprising: a translation unit

receiving the global motion parameters, and translating the global motion parameters

into a global motion vector which is in a form substantially identical to that of the

macroblock motion vector (Nakaya '6571: Equations (5), (6), (7), and (8); the vector

components are calculated from motion information parameters), and an interpolation

unit for receiving a decoded image which is a previously decoded frame, receiving the

selected macroblock motion vector or the selected global motion vector which is in a

form substantially identical to that of the macroblock motion vector outputted by the

multiplexer, performing interpolation operations, and generating the prediction image

(Nakaya '6571: Fig. 11; column 15, lines 2-8, either the global motion scheme or the

block matching scheme is employed based on the selection information extracted from

the motion information and the appropriate synthesizer feeds the predicted image into

the switch for output).

Nakaya '6571 does not specifically disclose a multiplexer selecting an inputted

macroblock motion vector or the inputted global motion vector which is in a form

substantially identical to that of the macroblock motion vector and outputting the

selected macroblock motion vector or the selected global motion vector which is in a

form substantially identical to that of the macroblock motion vector. However, Nakaya

'6571 does disclose a multiplexer with inputs connected to the GMC predicted image

synthesizer and the block matching predicted synthesizer (Nakaya '6571: Fig. 11,

multiplexer 908; column 15, lines 2-8, either the global motion scheme or the block matching scheme is employed based on the selection information extracted from the motion information and the appropriate synthesizer feeds the predicted image into the switch for output). Although the multiplexer disclosed by Nakaya '6571 inputs information from the synthesizer units, as opposed to the claimed outputting motion vector data to the interpolation unit, one of ordinary skill in the art at the time of the invention would have found it obvious that in both the claimed configuration and the configuration described by Nakaya '6571, the interpolation unit (embodied by the predicted image synthesizer 711 in Fig. 7 of Nakaya '6571) receives either a global motion vector or block motion vector and generates a predicted image. The configuration presented in the prior art, wherein the multiplexer selects from either the global motion predicted image or the block matching predicted image (Nakaya '6571: Fig. 11), inputs the appropriate vector type to the prediction units (Nakaya '6571: Fig. 11, elements 904 and 907) and selects the appropriate input for the multiplexer (Nakaya '6571: Fig. 11, element 909), assuring that the resultant predicted image is interpolated with the proper motion type, yielding the same results as the claimed configuration. Therefore, the surrounding elements in the decoding system, such as the decoder shown in Fig. 7 of Nakaya '6571, would function the same regardless of whether the predicted image synthesizer (Nakaya '6571: Fig. 7, element 711) conformed to the configuration shown in Fig. 11 of Nakaya '6571 or the configuration claimed in the instant application, and, thus, there would be no invention in shifting the position of the multiplexer, as claimed by the Applicant. See In re Japikse, 86 USPQ 70 (CCPA 1950).

Re **claim 25**, Nakaya '6571 discloses a demultiplexer receiving the macroblock motion vectors and global motion parameters, and respectively outputting the macroblock motion vectors and the global motion parameters, the global motion parameters are sent to the translation unit and translated into a global motion vector which is in a form substantially identical to that of the macroblock motion vector, and the interpolation unit selectively receiving the macroblock motion vector or the global motion vector to perform the interpolation operations (Nakaya '6571: column 14, line 54, through column 15, line 8).

Re **claim 26**, Nakaya '6571 discloses that the interpolation unit receives the global motion vector when a current macroblock is encoded using global motion compensation (Nakaya '6571: Equations (5), (6), (7), and (8); column 14, lines 58-64).

Re **claim 29**, Nakaya '6571 discloses that the interpolation unit receives the macroblock motion vector when a current macroblock is encoded using block-matching motion compensation (Nakaya '6571: Fig. 11; column 15, lines 2-8).

Re **claim 32**, Nakaya '6571 discloses performing interpolation using a representative global motion vector (Nakaya '6571: column 11, line 55, through column 12, line 19), wherein the corner points used in the calculations correspond to the corner points of a macroblock (Nakaya '6571: Fig. 1; column 2, lines 63-67).

Claim 33 has been analyzed and rejected with respect to claim 32 above.

Re **claim 34**, Nakaya '6571 discloses a majority of the features of claim 34, as discussed above in claim 24, but does not specifically disclose that the video decoder is for processing only an incoming MPEG-4 video stream having a

no_of_sprite_warping_point parameter set to either 0 or 1. However, The Examiner

takes Official Notice that when the number of sprite warping points is set to either 0 or 1,

the block either doesn't change position (set to 0) or is moved with respect to only one

motion vector without warping the boundaries of the block (set to 1). This qualifies as a

range of 0 to 1 sprite warping points, which is encompassed by the well-known range of

0 to 4 sprite warping points in MPEG-4 encoders and decoders. The Examiner notes

that the courts have long established that this modification of range is well within the

purview of one of ordinary skill in the art (See: In re Reven, 156 USPQ 679 (CCPA

1968)). Furthermore, the courts have established that "omission of an element and its

function in a combination is an obvious expedient if the remaining elements perform the

same functions as before." (See: In re Karlson, 136 USPQ 184 (CCPA 1963))

Therefore, the block behaves like that of an MPEG-1 or MPEG-2 block, which is well

known to one of ordinary skill in the art.

1.   Claims 5-8, 16-19, and 30-31 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Nakaya (US 7006571 B1, hereafter referred to as "'6571") as

applied to claims 1-4, 12-15, 23-26, 29, and 32-34 above, and further in view of

Nakaya et al. (US 20010050957 A1, hereafter referred to as "'50957").

Re **claim 5**, Nakaya '6571 does not specifically disclose that the interpolation

operations comprise luminance and chrominance interpolation operations. However,

Nakaya '50957 discloses interpolation using luminance and chrominance values

(Nakaya '50957: paragraphs [0012]-[0013]). Since Nakaya '6571 relates to decoding

images by processing motion vectors and Nakaya '50957 relates to preventing error

accumulation in image decoding, one of ordinary skill in the art would have found it

obvious to combine their teachings in order to improve the quality of the reproduced

picture by eliminating error accumulation.

Re **claim 6**, Nakaya '6571 does not specifically disclose that when performing

the luminance interpolation operations on macroblocks encoded using block-matching

motion compensation, the interpolation unit uses half-pel (or half-pixel) precision.

However, Nakaya '50957 discloses that, "the horizontal and vertical components of the

motion vector for the Y block motion vector are integral multiples of ½ (Nakaya '50957:

paragraph [0016])." This describes half pixel precision for the luminance (Y) block.

Since '6571 relates to decoding images by processing motion vectors and Nakaya

'50957 relates to preventing error accumulation in image decoding, one of ordinary skill

in the art would have found it obvious to combine their teachings in order to improve the

quality of the reproduced picture by eliminating error accumulation.

Re **claim 7**, Nakaya '6571 does not specifically disclose that when performing

the chrominance interpolation operations on macroblocks encoded using block-

matching motion compensation, the interpolation unit uses half-pel (or half-pixel)

precision. However, Nakaya '50957 discloses that the ¼ pixel resolution chrominance

blocks are rounded to ½ pixel precision (Nakaya '50957: paragraph [0016]). Since

Nakaya '6571 relates to decoding images by processing motion vectors and Nakaya

'50957 relates to preventing error accumulation in image decoding, one of ordinary skill

in the art would have found it obvious to combine their teachings in order to improve the quality of the reproduced picture by eliminating error accumulation.

Re **claim 8**, Nakaya '6571 does not specifically disclose that when performing the luminance interpolation operations on macroblocks encoded using global motion compensation, the interpolation unit uses half-pel (or half-pixel) precision. However, Nakaya '50957 discloses that, "the horizontal and vertical components of the motion vector for the Y block motion vector are integral multiples of ½ (Nakaya '50957: paragraph [0016])." This describes half pixel precision for the luminance (Y) block. Nakaya '50957 further discloses that this technique is applicable to global motion compensation in addition to block matching (Nakaya '50957: paragraph [0052]). Since Nakaya '6571 relates to decoding images by processing motion vectors and Nakaya '50957 relates to preventing error accumulation in image decoding, one of ordinary skill in the art would have found it obvious to combine their teachings in order to improve the quality of the reproduced picture by eliminating error accumulation.

Claim 16 has been analyzed and rejected with respect to claim 5 above.

Claim 17 has been analyzed and rejected with respect to claim 6 above.

Claim 18 has been analyzed and rejected with respect to claim 7 above.

Claim 19 has been analyzed and rejected with respect to claim 8 above.

Re **claim 30**, Nakaya '6571 does not specifically state that the interpolation operations include a luminance interpolation operation and a chrominance interpolation operation, the interpolation unit uses a first resolution to perform the luminance interpolation operation and uses a second resolution to perform the chrominance

interpolation operation. However, Nakaya '50957 discloses chrominance blocks in quarter pixel precision (Nakaya '50957: paragraph [0016]) and that this technique is applicable to global motion compensation in addition to block matching (Nakaya '50957: paragraph [0052]), but these blocks are rounded to the same precision as the luminance block in order to lessen the computational complexity of interpolation. Since Nakaya '6571 relates to decoding images by processing motion vectors and Nakaya '50957 relates to preventing error accumulation in image decoding, one of ordinary skill in the art would have found it obvious to combine their teachings in order to improve the quality of the reproduced picture by eliminating error accumulation.

Re **claim 31**, Nakaya '6571 discloses that when performing the interpolation operations, the interpolation unit uses a bilinear interpolation process (Nakaya '6571: column 3, lines 37-40).

2.   **Claim 9, 20, and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaya (US 7006571 B1, hereafter referred to as '"6571") and Nakaya et al. (US 20010050957 A1, hereafter referred to as '"50957") as applied to claims 1-8, 12-19, 23-26, and 29-31 above, and further in view of Srinivasan (US 20030202607 A1).**

Re **claim 9**, Nakaya '6571 does not specifically disclose that when performing the chrominance interpolation operations on macroblocks encoded using global motion compensation, the interpolation unit uses quarter-pel precision. Nakaya '50957 discloses chrominance blocks in quarter pixel precision (Nakaya '50957: paragraph

[0016]) and that this technique is applicable to global motion compensation in addition

to block matching (Nakaya '50957: paragraph [0052]), but these blocks are rounded to

half pixel precision in order to lessen the computational complexity of interpolation.

Srinivasan, however, discloses a sub-pixel interpolation technique in motion estimation

and compensation, which maintains the quarter pixel precision of the chrominance

blocks (Srinivasan: Fig. 18; paragraph [0183]). Since Nakaya '6571, Nakaya '50957,

and Srinivasan relate to image decoding utilizing motion compensation and interpolated

motion values, one of ordinary skill in the art at the time of the invention would have

found it obvious to combine their teachings in order to improve the image quality of the

reproduced picture.

   Claim 20 has been analyzed and rejected with respect to claim 9 above.

   Re **claim 27**, Nakaya '6571 does not specifically state that the interpolation

operations include a luminance interpolation operation and a chrominance interpolation

operation, the interpolation unit uses a first resolution to perform the luminance

interpolation operation and uses a second resolution to perform the chrominance

interpolation operation. Nakaya '50957 discloses chrominance blocks in quarter pixel

precision (Nakaya '50957: paragraph [0016]) and that this technique is applicable to

global motion compensation in addition to block matching (Nakaya '50957: paragraph

[0052]), but these blocks are rounded to the same precision as the luminance block in

order to lessen the computational complexity of interpolation. Srinivasan, however,

discloses a sub-pixel interpolation technique in motion estimation and compensation,

which maintains different resolutions for the luminance and chrominance blocks

(Srinivasan: Fig. 18; paragraph [0183]). Since Nakaya '6571, Nakaya '50957, and

Srinivasan relate to image decoding utilizing motion compensation and interpolated

motion values, one of ordinary skill in the art at the time of the invention would have

found it obvious to combine their teachings in order to improve the image quality of the

reproduced picture.

Re **claim 28**, Nakaya '6571 does not specifically state that the first resolution is a

half-pel resolution, and the second resolution is a quarter-pel resolution. Nakaya '50957

discloses chrominance blocks in quarter pixel precision (Nakaya '50957: paragraph

[0016]) and that this technique is applicable to global motion compensation in addition

to block matching (Nakaya '50957: paragraph [0052]), but these blocks are rounded to

the same precision as the luminance block in order to lessen the computational

complexity of interpolation. Srinivasan, however, discloses a sub-pixel interpolation

technique in motion estimation and compensation, which maintains the quarter pixel

precision of the chrominance blocks (Srinivasan: Fig. 18; paragraph [0183]). Since

Nakaya '6571, Nakaya '50957, and Srinivasan relate to image decoding utilizing motion

compensation and interpolated motion values, one of ordinary skill in the art at the time

of the invention would have found it obvious to combine their teachings in order to

improve the image quality of the reproduced picture.

3.   **Claims 10-11 and 21-22 are rejected under 35 U.S.C. 103(a) as being**

unpatentable over Nakaya (US 7006571 B1, hereafter referred to as "'6571") as

applied to claims 1-4, 12-15, 23-26, and 29 above, and further in view of Hagiwara

(US 20040223550 A1).

Re **claim 10**, Nakaya '6571 discloses that the decoder device that is intended for use with encoded bitstreams adhering to the MPEG-1, MPEG-2, and H.263 standards. However, Hagiwara discloses an MPEG-4 decoder, which includes the same principle processing steps of the MPEG-2 compliant decoder of Nakaya '6571. More specifically, Hagiwara includes a motion compensation block (Hagiwara: Fig. 11/8), which inputs a motion vector and reference frame and outputs a motion compensated reference frame to be added to the current frame being processed. Since both Nakaya '6571 and Hagiwara disclose MPEG compliant video decoders, one of ordinary skill in the art would have found it obvious at the time of the invention to combine their teachings in order to construct an MPEG-4 decoder which processes video with a very high compression rate.

Re **claim 11**, the combined decoder device of Nakaya '6571 and Hagiwara discloses a majority of the features of claim 11, as discussed above in claim 10, but does not specifically disclose that the video decoder is for processing only an incoming MPEG-4 video stream having a no_of_sprite_warping_point parameter set to either 0 or 1. However, The Examiner takes Official Notice that when the number of sprite warping points is set to either 0 or 1, the block either doesn't change position (set to 0) or is moved with respect to only one motion vector without warping the boundaries of the block (set to 1). This qualifies as a range of 0 to 1 sprite warping points, which is encompassed by the well-known range of 0 to 4 sprite warping points in MPEG-4

encoders and decoders. The Examiner notes that the courts have long established that

this modification of range is well within the purview of one of ordinary skill in the art

(See: In re Reven, 156 USPQ 679 (CCPA 1968)). Furthermore, the courts have

established that "omission of an element and its function in a combination is an obvious

expedient if the remaining elements perform the same functions as before." (See: In re

Karlson, 136 USPQ 184 (CCPA 1963)) Therefore, the block behaves like that of an

MPEG-1 or MPEG-2 block, which is well known to one of ordinary skill in the art.

   Claim 21 has been analyzed and rejected with respect to claim 10 above.

   Claim 22 has been analyzed and rejected with respect to claim 11 above.

Contact

   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to CHRISTOPHER FINDLEY whose telephone number is

(571)270-1199. The examiner can normally be reached on Monday through Friday,

8:30AM-5:00PM.

   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Marsha D. Banks-Harold can be reached on 571-272-7905. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

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